AMENDMENTS

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Original) An optoelectronic module, comprising:

a housing;

an optoelectronic component substantially disposed within the housing;

a controller IC disposed within the housing and including a serial digital interface configured to facilitate communication, between the optoelectronic module and a host, of diagnostic parameter information concerning the optoelectronic component; and

a pinout arrangement comprising:

a pin array having a plurality of pins, at least some of which are in communication with the controller IC; and

a pair of pins in communication with the serial digital interface, each of the pair of pins also being configured and arranged for communication with the host by way of a corresponding interface line.

2. (Original) The optoelectronic module as recited in claim 1, wherein the optoelectronic component comprises at least one of: a transmit optical subassembly; and, a receive optical subassembly.

3. (Currently Amended) The optoelectronic module as recited in claim 1, wherein the serial digital interface is compatible with one of[[.]]: I^2C serial communication; or, MDIO serial communication.

4. (Original) The optoelectronic module as recited in claim 1, wherein the controller IC is configured to receive from the host, by way of at least one of the pair of pins, at least one of the following: a command; data; and, diagnostic parameter information.

5. (Original) The optoelectronic module as recited in claim 1, wherein one of the pair of pins is configured to communicate with the host by way of an SDA interface line, and the other of the pair of pins is configured to communicate with the host by way of an SCL interface line.

6. (Currently Amended) The optoelectronic module as recited in claim 1, wherein the pin array is configured and arranged for substantial conformity with the SFF configuration standard in effect as of the filing date of the present application.

7. (Original) The optoelectronic module as recited in claim 1, wherein the pin array comprises one of: a 2x5 pin arrangement; and, a 2x10 pin arrangement.

8. (Original) The optoelectronic module as recited in claim 1, wherein the diagnostic parameter information includes at least one of: warning information; alarm information; and, status information.

9. (Original) The optoelectronic module as recited in claim 1, wherein one of the pair of pins comprises a serial communication data pin, and the other of the pair of pins comprises a serial communication clock pin.

10. (Original) The optoelectronic module as recited in claim 1, wherein the pair of pins is configured for repeated pluggability.

11. (Original) The optoelectronic module as recited in claim 1, wherein the controller IC is configured to generate at least one of: a temperature dependent output; and, a temperature independent output.

12. (Original) The optoelectronic module as recited in claim 1, wherein the controller IC further comprises an analog monitoring connection.

13. (Currently Amended) The optoelectronic module as recited in claim 1, wherein the serial digital interface substantially conforms to one of: a GBIC standard in effect as of the filing date of the present application; and, the SFF standard in effect as of the filing date of the present application.

14. (Original) The optoelectronic module as recited in claim 1, wherein the optoelectronic module is configured to receive a "rate select" signal from the host by way of one of the pins of the pinout arrangement.

15. (Original) The optoelectronic module as recited in claim 1, wherein the optoelectronic module is configured to transmit a "transmitter fault" signal to the host by way of one of the pins of the pinout arrangement.

16. (Original) The optoelectronic module as recited in claim 1, further comprising a plurality of memory mapped locations, at least one of which is accessible by way of the serial digital interface.

17. (Original) An optical transceiver module, comprising:

a housing;

a transmit optical subassembly substantially disposed within the housing;

a receive optical subassembly substantially disposed within the housing;

a controller IC disposed within the housing and including:

a serial digital interface configured and arranged to facilitate communication, between the optical transceiver module and a host, of diagnostic parameter information relating to at least one of: the transmit optical subassembly; and, the receive optical subassembly; and

a plurality of memory mapped locations, at least one of which is configured to store diagnostic parameter information and is accessible by way of the serial digital interface; and

a pinout arrangement comprising:

a pin array having a plurality of pins, at least some of which are in communication with the controller IC; and

a pair of pins in communication with the serial digital interface, each of the pair of pins also being configured and arranged for communication with the host by way of a corresponding interface line.

18. (Original) The optical transceiver module as recited in claim 17, wherein the serial digital interface is compatible with one of: I^2C serial communication; or, MDIO serial communication.

19. (Original) The optical transceiver module as recited in claim 17, wherein the controller IC is configured to receive from the host, by way of at least one of the pair of pins, at least one of the following: a command; data; and, diagnostic parameter information.

20. (Original) The optical transceiver module as recited in claim 17, wherein one of the pair of pins is configured to communicate with the host by way of an SDA interface

line, and the other of the pair of pins is configured to communicate with the host by way of an SCL interface line.

21. (Currently Amended) The optical transceiver module as recited in claim 17, wherein the pin array is configured and arranged for substantial conformity with the SFF configuration standard in effect as of the filing date of the present application.

22. (Original) The optical transceiver module as recited in claim 17, wherein the pin array comprises one of a 2x5 pin arrangement; and, a 2x10 pin arrangement.

23. (Original) The optical transceiver module as recited in claim 17, wherein the diagnostic parameter information includes at least one of: warning information; alarm information; and, status information.

24. (Original) The optical transceiver module as recited in claim 17, wherein one of the pair of pins comprises a serial communication data pin, and the other of the pair of pins comprises a serial communication clock pin.

25. (Original) The optical transceiver module as recited in claim 17, wherein the pair of pins is configured for repeated pluggability.

26. (Original) The optical transceiver module as recited in claim 17, wherein at least one of the plurality of memory mapped locations is implemented as a register.

27. (Original) The optical transceiver module as recited in claim 17, wherein at least one of the plurality of memory mapped locations is configured to be read, and written to, by way of the serial digital interface.

28. (Original) The optical transceiver module as recited in claim 17, wherein at least one of the memory mapped locations is configured to receive and store information concerning at least one of the following diagnostic parameters: a bias current associated with the transmit optical subassembly; optical transmit power associated with the transmit optical subassembly; received signal power; supply voltage; laser temperature; operation time; and, polarity and type of input and output signals.

29. (Original) The optical transceiver module as recited in claim 17, wherein the diagnostic parameter information stored in the at least one memory mapped location is in a digitized form.

30. (Original) The optical transceiver module as recited in claim 17, wherein the pin array comprises two rows of six pins each, each pin of the two rows of six pins comprising one of the following: a serial communication data pin; a receiver ground pin; a receiver power pin; a signal detect pin; a receive data inverted pin; a receive data pin; a serial communication clock pin; a transmitter power pin; a transmitter ground pin; a transmitter disable pin; a transmit data pin; a transmit data inverted pin; an interrupt pin; and a loss of signal pin.

31. (Original) The optical transceiver module as recited in claim 17, further comprising one or more of: a laser driver; a laser bias controller; a power controller; a preamplifier; a post-amplifier; a laser wavelength controller; a main controller; an electrothermal cooler; an analog-to-digital converter; a digital-to analog converter; and, an avalanche photodiode bias controller.

32. (Original) The optical transceiver module as recited in claim 17, wherein the optical transceiver module is configured to receive a "rate select" signal from the host by way of one of the pins of the pinout arrangement.

33. (Original) The optical transceiver module as recited in claim 32, wherein the "rate select" signal includes at least "high" and "low" values, each of which corresponds to a different data rate.

34. (Original) The optical transceiver as recited in claim 32, wherein the "rate select" signal is received from the host by way of one of the pair of pins.

35. (Original) The optical transceiver module as recited in claim 17, wherein the optical module is configured to transmit a "transmitter fault" signal to the host by way of one of the pins of the pinout arrangement.

36. (Original) The optical transceiver as recited in claim 35, wherein the "transmitter fault" signal is transmitted to the host by way of one of the pair of pins.

37. (Original) The optical transceiver module as recited in claim 17, wherein a memory map table associated with at least one of the plurality of memory map locations comprises information indicating at least one of: a storage location of a measured value of a diagnostic parameter; a storage location of a limit value for a diagnostic parameter; a storage location of a flag value for a diagnostic parameter; and, a storage location of a configuration value for a diagnostic parameter.

38. (Currently Amended) An optoelectronic module, comprising:

a housing;

an optoelectronic component substantially disposed within the housing;

a controller IC disposed within the housing and including a serial digital interface configured to facilitate communication, between the optoelectronic module and a host, of diagnostic parameter information concerning the optoelectronic component; and

a pinout arrangement comprising:

a pin array having a set of pins configured and arranged for substantial conformity with the SFF configuration standard in effect as of the filing date of the present application; and

a pair of pins in communication with the serial digital interface, each of the pair of pins also being configured and arranged for communication with the host by way of a corresponding interface line.

39. (Original) The optoelectronic module as recited in claim 38, wherein the optoelectronic component comprises at least one of: a transmit optical subassembly; and, a receive optical subassembly.

40. (Original) The optoelectronic module as recited in claim 38, wherein the serial digital interface is compatible with one of: I^2C serial communication; and MDIO serial communication.

41. (Original) The optoelectronic module as recited in claim 38, wherein the controller IC is configured to receive from the host, by way of one at least one of the pair of pins, at least one of the following: a command; data; and, diagnostic parameter information.

42. (Original) The optoelectronic module as recited in claim 38, wherein one of the pair of pins is configured to communicate with the host by way of an SDA interface line,

and the other of the pair of pins is configured to communicate with the host by way of an SCL interface line.

43. (Original) The optoelectronic module as recited in claim 38, wherein the pin array comprises one of: a 2x5 pin arrangement; and, a 2x10 pin arrangement.

44. (Original) The optoelectronic module as recited in claim 38, wherein the diagnostic parameter information comprises at least one of: warning information; alarm information; a measured value of a diagnostic parameter; a limit value associated with a diagnostic parameter; a flag value associated with a diagnostic parameter; a configuration value associated with a diagnostic parameter; a bias current associated with the optoelectronic component; an optical transmit power associated with the optoelectronic component; and, a received signal power associated with the optoelectronic component.

45. (Original) The optoelectronic module as recited in claim 38, wherein one of the pair of pins comprises a serial communication data pin, and the other of the pair of pins comprises a serial communication clock pin.

46. (Original) The optoelectronic module as recited in claim 38, further comprising a plurality of memory mapped locations, at least one of which is accessible by way of the serial digital interface and which is configured to receive and store information concerning at least one diagnostic parameter.

47. (Previously Presented) The optoelectronic module as recited in claim 1, wherein the pin array includes the pair of pins such that the pair of pins is used for multiple and different types of signals, at least one of which is digital parameter information.

48. (Previously Presented) The optoelectronic module as recited in claim 1, wherein the pin array has a plurality of pins arranged in two rows, and the pair of pins is not aligned with either of the two rows.

49. (Previously Presented) The optoelectronic module as recited in claim 1, further comprising:

memory; and

a memory interface for allowing a host device to read from and write to memory mapped locations within the memory in accordance with commands received from a host device, wherein the memory interface allows the host device to read digital values corresponding to the diagnostic parameter information from the memory mapped locations through the pair of pins.

50. (Previously Presented) The optoelectronic module as recited in claim 38, wherein the pin array includes the pair of pins such that the same pair of pins is used for multiple and different types of signals, at least one of which is digital parameter information.

51. (Previously Presented) The optoelectronic module as recited in claim 38, wherein the pin array has plurality of pins arranged in two rows, and the pair of pins is not aligned with either of the two rows.

52. (Previously Presented) The optoelectronic module as recited in claim 38, further comprising:

memory; and

a memory interface for allowing a host device to read from and write to memory mapped locations within the memory in accordance with commands received from a host device, wherein the memory interface allows the host device to read

digital values corresponding to the diagnostic parameter information from the memory mapped locations through the pair of pins.

53. (New) An optoelectronic module, comprising:

a housing;

an optoelectronic component substantially disposed within the housing;

analog-to-digital conversion circuitry configured to receive a plurality of analog signals from the optoelectronic component, the analog signals corresponding to operating conditions of the optoelectronic component, convert the received analog signals into digital values, and store the digital values in predefined memory-mapped locations;

comparison logic configured to compare the digital values with limit values to generate flag values, wherein the flag values are stored in predefined memory-mapped flag storage locations during operation of the optoelectronic component;

a serial digital interface configured to enable a host to read from host-specified memory-mapped locations, including the predefined memory-mapped flag storage locations; and

a pinout arrangement comprising:

a pin array having a plurality of pins; and

a pair of pins in communication with the serial digital interface, each of the pair of pins also being configured and arranged for communication with the host by way of a corresponding interface line.